Mechanism of Power Density Degradation due to Trapping Effects in AlGaN/GaN HEMTs

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Abstract — **AlGaN/GaN HEMTs are promising devices for very high power applications. These transistors present high breakdown voltages and have already shown their ability to operate at high temperature. But their power performances are limited because of the presence of traps within the material, decreasing the drain current density. In order to predict the loss of power density and quantify trapping effects, simulations need to be performed with a suited model, which accounts for these parasitic trapping effects. This paper deals with the characterization, modeling and simulation of trapping effects and power behavior of a 1mm GaN device on SiC substrate. Experimental results are compared to the simulations.**

I. Introduction

The wide band-gap materials such as GaN have already shown good performances for microwave high power applications [1]. The transistors made out of these materials, such as AlGaN/GaN HEMTs, present a high breakdown voltage and the ability to operate at high frequency and high temperatures. Although they are promising devices for high power wide band applications, considerable trapping effects remain and limit the performances of these transistors [2]. These parasitic effects act by decreasing the actual maximum output drain current and voltage swing in microwave applications [3]. As a consequence, the microwave power density of these devices is degraded.

In order to observe the parasitic effects due to traps, it is necessary that the different parasitic phenomena could be separately modeled and analyzed. This paper explains how to do so through dedicated pulsed measurement techniques, which are performed to quantify the influence of traps on I-V characteristics. The pulsed S-parameters have also been measured in order to derive a suited model for a 1mm GaN HEMT on SiC substrate. This model enables to efficiently compare the simulated and measured load-pull analysis results and to assess its ability to predict the power density degradation due to parasitic trapping effects within the device.

II. Highlight Trapping Effects Through Pulsed Measurements

The dispersion effects due to traps in AlGaN/GaN HEMTs are complex phenomena depending on many parameters [4] such as: the input and output quiescent bias conditions (Vgs_0, Vds_0), the input and output electrical field variations (ΔVgs, ΔVds), and the width and recurrence of the pulses used for the characterization.

As the quiescent bias conditions set the thermal and trapping state, they have to remain constant during the I-V acquisition. Then, several characteristics at different quiescent bias points are measured and compared in order to observe the influence of traps. These parasitic effects have to be highlighted during measurements in order to derive a suited model [5], which includes their critical influence. Indeed, when microwave large signals are applied to the device and explore its whole I-V characteristic, these parasitic effects significantly affect the actual device behavior.

A. Characterization of Gate-lag phenomenon

The gate-lag phenomenon has been associated to surface traps, which induce a transient drain current response leading to time delay in microwave circuits. This effect can be observed by looking at the influence of the gate to source voltage variation on the measured drain current.

In order to do so, the device needs to be characterized twice, at two different quiescent bias points. Moreover, its thermal state has to remain the same during the two experiments, which can be done by imposing a dissipated power equal to zero through the quiescent bias point (Vds_0=0). Doing so allows setting the device into two different trapping states but in the same thermal state. This way, the electrical field related to the gate to source voltage (ΔVgs) could considerably vary for the same operating point (Fig. 1-a). As this is the only parameter that changes between the two experiments, it allows to separately observing the influence of the gate-lag.

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B. Characterization of Self-backgating phenomenon

The self-backgating phenomenon is related to the dispersion effect due to traps within the semi-insulating substrate. This effect is due to the electrical field generated by the drain to source voltage. It can be observed by looking at the influence of drain to source voltages on the measured drain current. This analysis consists on the reverse experiment than the one done to highlight the gate-lag phenomenon; that is to say a fixed value of Vgs_0 at the pinch-off value and a changing value of the quiescent bias point Vds_0 (Fig. 1-b).

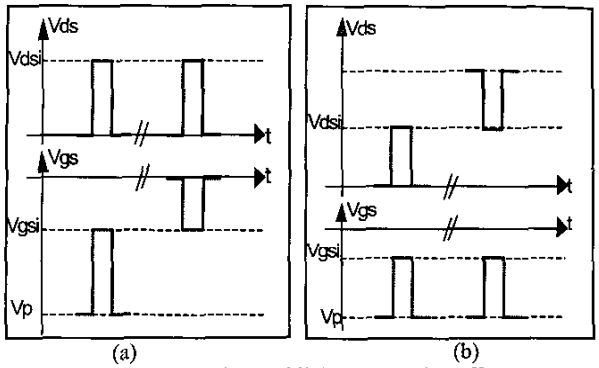

Fig. 1. Pulsed method to highlight the trapping effects: (a) Gate-lag phenomenon ; (b) Self-backgating phenomenon.

III. Measurement Results On A 1mm GaN Device On SiC Substrate

A. I-V characteristics

Pulsed measurements have been performed on a multi-fingers 1mm device on SiC wafer processed by Ferdinand-Braun-Institut in Berlin. The transistor is a GaN HEMT with a gate width of 125µm, a gate length of 0.3µm, and a gate pitch of 50µm. It was characterized through 450ns pulses using 6µs duty cycle. The pulsed I-V characteristics have been measured up to 50V of Vds, and the pulsed S-parameters up to 40GHz. The pinch-off voltage is -3.5V, and a drain current density of 900mA/mm is obtained at the quiescent bias point (Vgs_0=0V, Vds_0=0V) (Fig. 2.). At the operating point (Vgsi=-2V, Vdsi=26.4V, Idi=199mA), the measured device exhibits 7dB maximum gain at 20GHz, over 50GHz maximum oscillation frequency, and 31GHz cutoff frequency.

B. Presence of traps

The measurement experiments described earlier in this paper to highlight the gate-lag and self-backgating phenomena have been performed on the device.

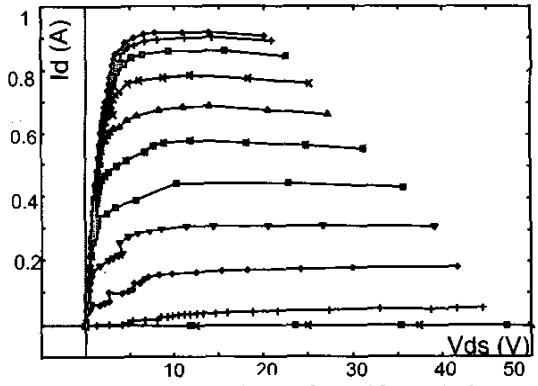

Fig. 2. Id-Vds characteristic of 8x125µm device at the quiescent bias point (Vgs_0=0V, Vds_0=0V) for a drain to source voltage up to 50V and a gate to source voltage swept from –4V to +1.5V in steps of 0.5V.

I-V characteristics have been measured at different quiescent bias points. Figure 3 shows the comparison of the I-V characteristics measured at (Vgs_0=-4V, Vds_0=0V) and (Vgs_0=0V, Vds_0=0V). The difference between these two characteristics is due to the influence of the gate to source bias voltage related to the gate-lag phenomenon. The surface traps act on the drain current by leading to a drastic decrease. As a consequence, the microwave signal will be significantly affected by this decrease, which lowers its swing and limits the device output power.

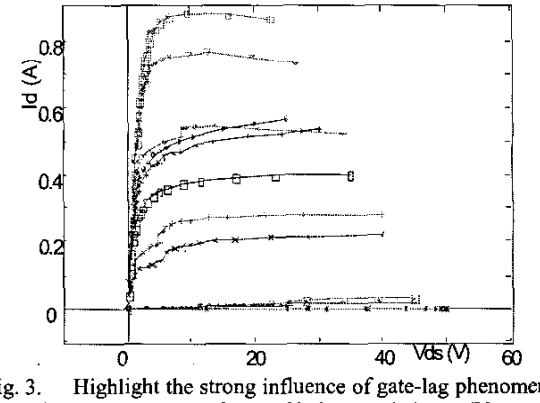

Fig. 3. Highlight the strong influence of gate-lag phenomenon through the comparison of two I-V characteristics at (Vgs_0=-4V, Vds_0=0V) (dark color) and (Vgs_0=0V, Vds_0=0V) (fair color) for Vgs swept from –4V to +1V.

Figure 4 shows the comparison of the I-V characteristics measured at (Vgs_0=-4V, Vds_0=0V) and (Vgs_0=-4V, Vds_0=25V). The observed differences are due to the influence of the drain to source bias voltage, highlighting both the self-backgating and gate-lag phenomena. It can be noticed that the substrate traps act on the drain current within the linear zone of the I-V characteristic.

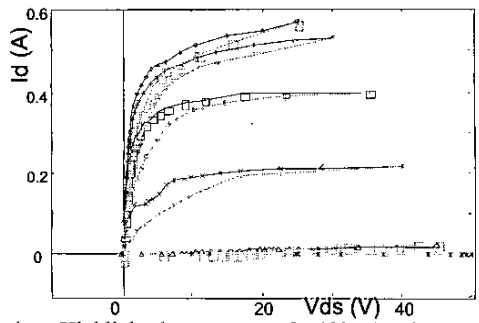

Fig. 4. Highlight the presence of self-backgating phenomenon through the comparison of two I-V characteristics at (Vgs_0=-4V, Vds_0=0V) (dark color) and (Vgs_0=-4V, Vds_0=25V) (fair color) for Vgs swept from –4V to +1V.

IV. Modeling And Simulation Of A 1mm GaN Device

A. Load-pull measurement results

Load-pull measurements have been performed on the 8x125µm device at the Ferdinand-Braun-Institut. The experiment has been done at (Vgsi=-2.2V, Vdsi=25V) bias point, 2GHz operating frequency, and (40Ω+j38Ω) output load at the fundamental frequency. The input power was swept up to 45mW. At 23.5mW input power, the device exhibits 2.5W output power, and 39.3% power added efficiency. As the device width is 8x125µm, it corresponds to a power density of 2.5W/mm.

B. Comparison of measured and simulated power results

1- Modeling at a cold quiescent bias point

A first model of the 8x125µm device has been derived with the help of dedicated modeling software developed at the IRCOM laboratory. The quiescent bias state considered is (Vgs_0=0V, Vds_0=0V) at which the traps do not present any huge effects. The extrinsic and intrinsic parameters obtained for a hot instantaneous bias point (Vgsi=-2V, Vdsi=27.8V) are shown in Table 1.

Rg (Ω)	Lg (pH)	Cpg (fF)	Rd (Ω)	Ld (pH)	Cpd (fF)	Rs (Ω)	Ls (pH)
1.97	192	66.7	2.5	185	95.5	0.9	4.32
Cgs (pF)	Cgd (fF)	Gm (mS)	gd (mS)	Cds (fF)	Ri (Ω)	Tau (ps)	Rgd (Ω)
1.60	60	361	8.73	279	5.24	2.18	197

Table 1. Extrinsic and intrinsic elements of the 8x125µm model derived at (Vgsi=-2V, Vdsi=27.8V) instantaneous bias point for a cold quiescent bias point (Vgs_0=0V, Vds_0=0V).

A dedicated fitting algorithm developed at the IRCOM laboratory and based on spline equations permitted to derive an accurate current source model of the device. Finally, the whole non-linear electrical model of the 8x125µm device has been implemented in the simulation software to compare measured and simulated S-parameter and power behaviors.

A good agreement is obtained between the measured and simulated S-parameters at the specified quiescent and instantaneous bias points (Fig. 5).

Figure 6 shows the comparison between the simulation and the measurement results of a load-pull experiment.

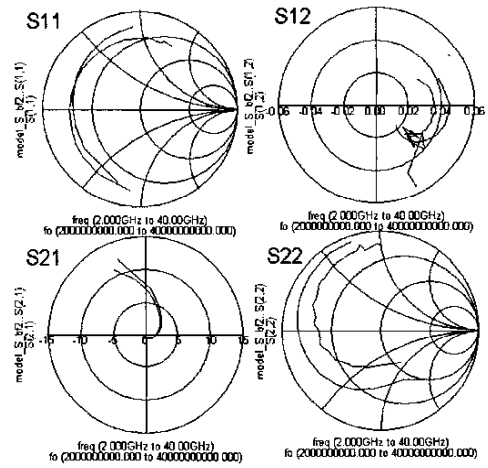

Fig. 5. Comparison between measured and simulated S-parameters from 2 to 40GHz at a cold quiescent bias point and (Vgs_0=-2V, Vds_0=27.8V) instantaneous bias point.

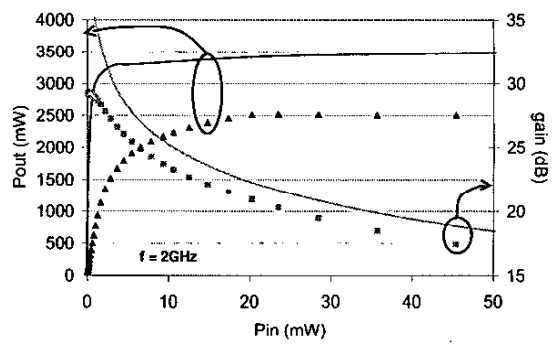

Fig. 6. Load-pull results: measured (dots) / simulated (lines)

In the specific case of this non-linear model biased at 0V quiescent point, and hence for which trapping effects are not included, Figure 6 shows a huge difference between the simulated and measured power results, meaning that neglecting the trap influence during device characterization and modeling leads to very inaccurate power predictions. Indeed, such a classical model, which does not take into account the loss of drain current density, is unable to predict the loss of power density.

2- Modeling at (-2.2V, 25.9V) quiescent bias point

In the same way, at the same instantaneous bias point (Vgsi=-2V, Vdsi=26.4V), another device model was derived but the quiescent bias state imposed during measurements was (Vgs_0=-2.2V, Vds_0=25.9V), which induces a drastic decrease of the measured drain current as illustrated earlier. The intrinsic parameters obtained are shown in Table 2 –the extrinsic parameters remain the same than for the model at a cold quiescent bias point.

A good agreement is obtained between the measured and simulated S-parameters at the specified quiescent and instantaneous bias points (Fig. 7).

Cgs (pF)	Cgd (fF)	Gm (mS)	gd (mS)	Cds (fF)	Ri (Ω)	Tau (ps)	Rgd (Ω)
1.45	40	267	6.72	267	6.15	2.04	163

Table 2. Intrinsic elements of the model at the instantaneous bias point (Vgsi=-2V, Vdsi=26.4V) for the quiescent bias point (Vgs_0=-2.2V, Vds_0=25.8V).

The cold and biased S-parameters measurements are pretty much identical (Fig.7), which demonstrates that considering only the S-parameters doesn't allow to express the trapping effects.

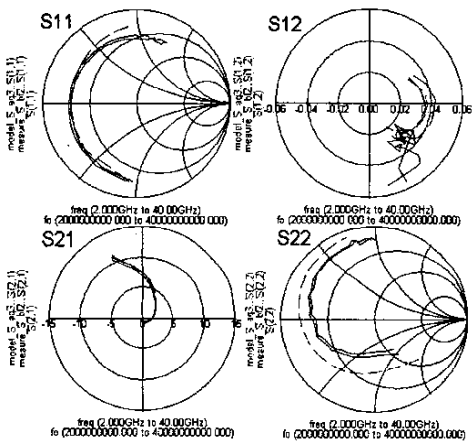

Fig. 7. Comparison between cold and biased measurements (solid lines) and simulated (long dash line) S-parameters from 2 to 40GHz at (Vgs_0=-2.2V, Vds_0=25.8V) quiescent bias point and (Vgsi=-2V, Vdsi=26.4V) instantaneous bias point.

Figure 8 shows the comparison between the simulation and the measurement results of a load-pull experiment. This figure shows a really good agreement between simulated and measured power results. This experiment demonstrates the importance of including the parasitic trapping effects within the model to accurately predict the actual power behavior, which is considerably influenced and degraded by trapping effects. In the particular case of the GaN device considered in this paper, trapping effects leads to approximately 30% loss in power density.

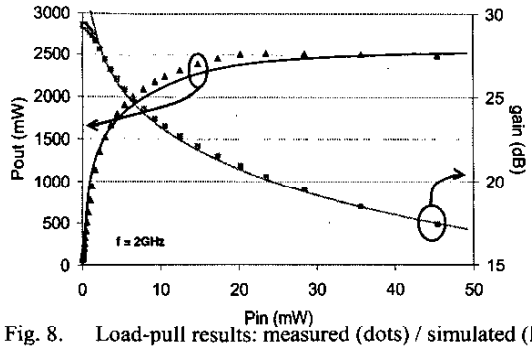

Fig. 8. Load-pull results: measured (dots) / simulated (lines)

V. Conclusion

Wide-band gap transistors are promising devices for very high power applications at microwave frequencies but presently limited by strong trapping effects. This paper deals with dedicated measurement and modeling techniques of trapping effects applied to a 1mm GaN HEMT on SiC substrate. Two non-linear models have been derived with and without accounting for trapping effects during I-V measurements. Power measurements at 2GHz have been performed to demonstrate the accuracy of the non-linear model, which includes trapping effects, and to assess the actual power degradation due to these parasitic effects.

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References

[1] S.T. Sheppard *et al.*, "High-power microwave GaN/AlGaN HEMT's on semi-insulating silicon carbide substrates," *IEEE Electron Devices Letters*, vol. 20, pp161-163, 1999.

[2] S. C. Binari *et al*, "Trapping effects in GaN and SiC microwave FETs," *Proceedings of the IEEE*, vol. 90, no. 6, pp. 1048-1058, June 2002.

[3] C. Nguyen *et al*, "Drain current compression in GaN MODFETs under large-signal modulation at microwave frequencies," *Electronics Lett.*, vol. 35, no. 16, Aug 1999.

[4] J.-P. Teyssier *et al*, "40-GHz/150-ns versatile pulsed measurement system for microwave transistor isothermal characterization," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no. 12, pp. 2043-2052, December 1998.

[5] D. Siriex *et al*, "Characterization and modeling of nonlinear trapping effects in power SiC MESFETs," *Microwave Symposium Digest, 2000 IEEE MTT-S International*, vol. 2, pp. 765-768, 2002.